What is claimed is:

1. A method, comprising:

receiving, via a first communications medium, a first file including programmable logic instructions in a non-native format;

converting said non-native format programmable logic instructions into programmable logic instructions having a format native to said remote programmable logic device; and

transmitting to said remote programmable logic device, via a second communications medium, a second file including said native format programmable logic instructions.

2. The method of claim 1, wherein said first communications medium comprises an Ethernet network.

3. The method of claim 1, wherein said second communications medium comprises an inter-circuit board bus communicating between a processing element and said remote programmable logic device.

4. The method of claim 1, wherein said native format comprises a JTAG format.

5. The method of claim 1, further comprising the steps of causing said programmable logic device to enter an initial operating state.

6. A method for programming a remote programmable logic device, comprising:

sending a first file to a processing system via a first communications medium;

converting said first file to a second file in a format native to said remote programmable logic device; and

sending said second file in a format native to said remote programmable logic device to said remote programmable logic device via a second communications medium.

7. The method of claim 6 wherein sending said first file further comprises the step of transferring said first file via an Ethernet network.

8. The method of claim 6 wherein said converting said first file to a second file further comprises the steps of processing said first file with a file conversion program via a processor.

9. The method of claim 8 wherein said converting said first file to a second file further comprises the steps of storing said second file in a format native to said remote programmable logic device in a buffer.

10. The method of claim 6 wherein said sending said second file further comprises transferring said second file over an inter-board bus to said remote programmable logic device.

11. The method of claim 6 wherein said converting step further comprises converting said first file into a JTAG format.

12. The method of claim 6 further comprising the steps of:

powering down the remote programmable logic device; and

powering on the remote programmable logic device.

13. An apparatus for programming a remote programmable logic device, comprising:

a processing system having a first file to second file conversion program stored therein; said processing system receiving said first file from a first communications medium and transmitting said converted second file through a second communications medium in a format native to said remote programmable logic device.

14. The apparatus of claim 13 wherein said first communications medium is an Ethernet network.

15. The apparatus of claim 13 wherein said second communications medium is an inter-board input/output bus.

16. The apparatus of claim 13 wherein said format native to said remote programmable logic device is a JTAG format.

17. The apparatus of claim 13 wherein said processing system further comprising a processor coupled to said buffer wherein said processor executes said first file to second file conversion program.

18. The apparatus of claim 17 further comprising a buffer coupled to said processor for storing said second file in a format native to said remote programmable logic device.

19. An apparatus for programming a field programmable gate array, comprising:

a processing system having a first file to second file conversion program stored therein; said processing system receiving said first file from a first communications medium and transmitting said converted second file through

a second communications medium in a format native to said remote programmable logic device.

20. The apparatus of claim 19 wherein said first file is a POF file.

21. The apparatus of claim 19 wherein said first communications medium is an Ethernet network.

22. The apparatus of claim 19 wherein said second communications medium is an inter-board input/output bus.

23. The apparatus of claim 19 wherein said format native to said remote programmable logic device is a JTAG format.

24. The apparatus of claim 19 wherein said processing system further comprising a processor coupled to said buffer wherein said processor executes said first file to second file conversion program.

25. The apparatus of claim 24 further comprising a buffer coupled to said processor for storing said second file in a format native to said remote programmable logic device.

26. A computer readable medium having computer executable instructions for performing steps comprising:

receiving, via a first communications medium, a first file including programmable logic instructions in a non-native format;

converting said non-native format programmable logic instructions into programmable logic instructions having a format native to said remote programmable logic device; and

transmitting to said remote programmable logic device, via a second communications medium, a second file including said native format programmable logic instructions.

27. A method for programming one or more programmable logic devices, comprising:

programming a first file in a non-native format for programming said one or more programmable logic devices from a remote programmer source;

converting said non-native format programmable logic instructions into a second file having programmable logic instructions in a format native to said remote programmable logic device;

transmitting to said remote programmable logic device, via a communications medium, said second file having said native format programmable logic instructions;

executing said converted file to selectively locate said one or more programmable logic devices via a first bus; and

programming said one or more selected programmable logic devices via a second bus.

28. The method of claim 27 wherein said first file is a programmer object file.

29. The method of claim 27 wherein said remote programmer source is selected from the group comprising a workstation, and a personal computer.

30. The method of claim 27 wherein said second file is a JAM byte code file.

31. The method of claim 27, wherein said communications medium is an Ethernet network.

32. The method of claim 27, wherein said native format comprises a JTAG format.

33. The method of claim 27, wherein said first bus is a board select bus.

34. The method of claim 27, wherein said second bus is a JTAG bus.

35. The method of claim 27 further comprising the step of causing said programmable logic device to enter an initial operating state.

36. A method for programming at least one programmable logic device, comprising:

receiving at a head-end controller via a first communications medium, a file having a format native to said at least one programmable logic device;

sending said native format file to a processor system via a second communications medium;

executing, via a processor, said native format file to identify and selectively access said at least one programmable logic device via a board select bus; and

programming said selectively accessed programmable logic devices via a JTAG bus.

37. The method of claim 36 wherein receiving said file further comprises the step of receiving said file via a telecommunications medium selected from the group comprising a LAN connection, a WAN connection, and Internet.

38. The method of claim 36 wherein receiving said file further comprises the step of receiving said file via a physical storage medium.

39. The method of claim 36 wherein sending said file further comprises the step of transferring said first file via an Ethernet network.

40. The method of claim 36 wherein said file is a JAM byte code file.

41. The method of claim 36, wherein said native format comprises a JTAG format.

42. The method of claim 36, wherein said first bus is a board select bus.

43. The method of claim 36, wherein said second bus is a JTAG bus.

44. The method of claim 36 wherein said at least one programmable logic device is respectively accessed via at least one respective switching circuit coupled to said processor via said first and second buses.

45. The method of claim 36 wherein prior to said receiving step, said method further comprises the steps of:

programming a first file in a non-native format of said at least one programmable logic device;

converting said non-native format file into said native format file; and

transmitting said native format file to said head-end controller via a communications medium.

46. The method of claim 36 further comprising the step of initializing said at least one programmable logic device to an operating state.

47. The method of claim 46 wherein said initializing step further comprising the step of recycling power to said at least one programmable logic device.

48. An apparatus for programming at least one programmable logic devices, comprising:

at least one circuit board respectively comprising said at least one programmable logic device coupled to at least one switching circuit; and

a processor system coupled to said at least one switching circuit via a board select bus and a JTAG bus; and

wherein said processor system executes a file in a format native to said at least one programmable logic device, enables said at least one switching circuit via the board select bus, and programs said at least one programmable logic device via said JTAG bus.

49. The apparatus of claim 48 wherein said first and second bus is a backplane.

50. The apparatus of claim 48 wherein said format native to said remote programmable logic device is a JTAG format.

51. The apparatus of claim 48 wherein said format native file is a JAM byte code file.

52. The apparatus of claim 48 wherein said at least one programmable logic device is selected from the group comprising a gate array, field programmable gate array,

programmable, field programmable logic array, read only memory, programmed array logic, programmable logic array, and complex programmable logic devices.

53. The apparatus of claim 48 wherein processor system is a server.

54. The apparatus of claim 48 wherein processor system is a switch.